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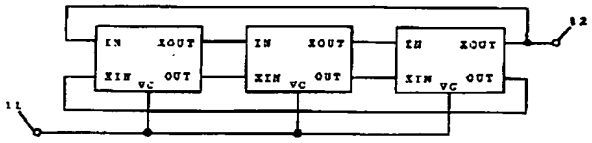
(54)【発明の名称】　電圧制御型発振回路

(57)【要約】

【目的】低電源電圧動作で高周波発振を安定に出力する電圧制御発振回路を実現する。また、雑音の低減やダイナミック特性の向上も図る。

【構成】複数の差動増幅器を用いた電圧制御発振回路。互いに前後する差動増幅器の差動電圧入力端子と差動出力端子が、互いの動作極性が反対となるように直列かつリング状に接続されている。また、全ての差動増幅器の電流制御入力端子は互いに接続されて電圧制御発振回路の制御入力端子１１となっている。１２は電圧制御型発振回路の出力端子である。なお、この出力端子は電圧制御発振回路を構成する任意の差動増幅器のいずれの出力端子でもよい。また、差動増幅器出力端子の一方を用いてシングルエンド出力としているが、差動増幅器の差動出力端子両方を用いて差動出力としてもよい。また、複数の差動増幅器の出力を同時に複数の出力端子として用いてもよい。



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【特許請求の範囲】

【請求項１】一対の差動電圧入力端子と一対の差動電圧出力端子を具備し、該差動電圧入力端子間に入力される差動電圧を増幅した結果を該差動出力端子間に差動出力する差動増幅器であって、該差動増幅器は差動増幅の動作電流が制御入力端子の入力によって制御される差動増幅器を具備し、該差動増幅器を複数個用いて互いに前後する差動増幅器の差動電圧入力端子と差動出力端子が互いの動作極性が反対となるように、直列かつリング状に接続したことを特徴とする電圧制御型発振回路。

【請求項２】請求項１記載の電圧制御型発振回路であって、該差動増幅器の電流制御入力端子を互いに接続し、該制御入力端子を入力とし、該差動増幅器の任意の単一もしくは複数の出力端子を出力としたことを特徴とする電圧制御型発振回路。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は電圧制御型発振回路に関するものである。

【０００２】

【従来の技術】従来の電圧制御型発振回路は例えば図３に示されるように反転回路をリング発振器として構成下ものであり、１つの反転回路のＶＤＤ側とＶＳＳ側に各々１個の電流制御トランジスタを挿入し、制御入力端子１１に入力される制御電圧によって２つの電流制御トランジスタに流れる電流を同時に制御することによって発振周波数を制御するというものであった。

【０００３】

【発明が解決しようとする課題】従来の電圧制御型発振回路における各反転回路の動作電流は該反転回路の入力電圧の関数であり一定ではない。これはＣＭＯＳ反転回路の動作原理からも明白である。よって、発振動作中に電流制御トランジスタ２１および２２に流れる電流も一定ではなく発振周波数の２倍の頻度で反転回路に流れる貫通電流がパルス状に流れることになる。従って、電流制御トランジスタ２１および２２はパルス電流が流れる瞬間のみの定電流飽和領域動作を要求され、その瞬間以外は非飽和領域動作状態となっている。

【０００４】ここで、２１および２２のドレイン端子である２３と２４を見ると、以上の理由からこれらの端子電圧も発振周波数の２倍の頻度でパルス状に振られることになる。所望の発振周波数が比較的低い場合は特に問題とはならないが、より高周波数で発振させようとすると、新たに次の問題が発生した。

【０００５】同じ制御電圧で発振周波数を上げるためには２１と２２の電流制御トランジスタの電流能力を大きくして動作電流を大きくすればよいが、通常このためには該トランジスタの物理寸法の増大が伴い、これに比例して２３と２４における寄生容量の増大を招く。前述の通り２３と２４は発振周波数の２倍の頻度で電圧が振られるため、ここの寄生容量が大きいと高速な電圧変化を妨げるため寄生容量は発振周波数を下げる方向に作用することになる。以上から発振周波数を上げようとして電流制御トランジスタの電流能力を上げても発振周波数は前記寄生容量によって低く制限されることになり、さらに寄生容量に流れる電流が原因となって反転回路の動作電流に対する発振周波数の直線性も損なわれるという問題が発生した。

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【０００６】また、従来の電圧制御型発振回路においては電源間に４個のトランジスタが直列に接続されるため、各トランジスタの端子間電圧を確保するために電源電圧をある電圧値以下にできないという問題があり、近年の低電源電圧化に充分に対応することができない。さらに、前述の通り電流制御トランジスタが１反転回路につき２個あるため、２０の制御電圧変換回路が別途必要となりこれは以下の問題を持つ。

【０００７】従来の電圧制御型発振回路の制御入力１１にＡＣ信号を入力すると電流制御トランジスタ２２のゲート端子にはそのまま伝わるが、電流制御トランジスタ２１のゲート端子には制御電圧変換回路２０を通ってから伝わるため、２２と２１のゲート端子間に制御電圧の時間的ずれが生じてしまう。また、１１を充分な低インピーダンスで駆動しても制御電圧変換回路２０の出力インピーダンスを消費電流の観点からあまり小さくできないため、制御電圧変換回路２０の出力が発振器からの影響を受け易くなり、全体の発振周波数の安定度を上げにくいという問題がある。

【０００８】さらに、前述の通り各反転回路には発振周波数の２倍の頻度でパルス状の貫通電流が流れているため、発振周波数を上げるほど電源のインピーダンスを充分低くしないと電源に雑音を重畳して他の回路あるいは自分自身に電源雑音の影響を及ぼして、発振の安定度を損ない易いという問題が発生した。

【０００９】

【課題を解決するための手段】一対の差動電圧入力端子と一対の差動電圧出力端子を具備し、該差動電圧入力端子間に入力される差動電圧を増幅した結果を該差動出力端子間に差動出力する差動増幅器であって、該差動増幅器は差動増幅の動作電流が制御入力端子の入力によって制御される差動増幅器を具備し、該差動増幅器を複数個用いて互いに前後する差動増幅器の差動電圧入力端子と差動出力端子が互いの動作極性が反対となるように直列かつリング状に接続することを特徴とする。また該差動増幅器の電流制御入力端子を互いに接続してこれを入力とし、該差動増幅器の任意の出力端子を出力としたことを特徴とする。

【００１０】

【実施例】図１に３個の差動増幅器を用いた本発明の電圧制御型発振回路の一実施例を示す。１は差動増幅器でありＣＭＯＳトランジスタで構成した場合の例を図２に

示す。２および３は差動入力端子であり４および５は差動出力端子である。６は電流制御入力端子であり、この端子に入力する電圧によって該作動増幅器の動作電流を制御する。この差動増幅器の動作は周知であるので説明を省略する。

【００１１】図１の電圧制御型発振回路は互いに前後する差動増幅器の差動電圧入力端子と差動出力端子が互いの動作極性が反対となるように直列かつリング状に接続し、該差動増幅器がリング発振器を構成するように接続されている。また、３個の差動増幅器の電流制御入力端子は互いに接続されて電圧制御型発振回路の制御入力端子１１となっている。１２は電圧制御型発振回路の出力端子である。なお、出力端子は電圧制御型発振回路を構成する任意の差動増幅器のいずれの出力端子でもよく、また図１では差動増幅器出力端子の一方を用いてシングルエンド出力としているが、差動増幅器の差動出力端子両方を用いて差動出力としてもよい。また、複数の差動増幅器の出力を同時に複数の出力端子として用いてもよい。

【００１２】本発明の電圧制御型発振回路の発振状態における差動増幅器１の動作状態について以下に述べる。差動入力トランジスタ９および１０には差動入力端子２および３の入力電圧に対応した電流が流れるが、両電流の和が７の電流制御トランジスタに流れる。ここで７の電流制御トランジスタが６の制御入力に与えられた直流電圧によって飽和領域における定電流動作をしているものとすると、７の電流制御トランジスタにはほぼ一定の直流電流が流れる。したがって、７の電流制御トランジスタのドレイン端子８の電圧も従来の電圧制御型発振回路のようにパルス状に急峻に変化することなく、ほぼ一定の電圧値で安定する。７の電流制御トランジスタの飽和領域動作のみを使用するように１の差動増幅器の構成と６の制御入力電圧範囲の最適化を図ることは８の電圧がほぼ一定であるので容易である。

【００１３】８の電圧がほぼ一定であるので端子８における寄生容量を高速に充放電する必要がないことから、該寄生容量の影響が小さくなる。これによって、電流制御トランジスタ７に流れる動作電流に対する発振周波数が上がり直線性も向上する。さらに、電圧制御型発振回路全体の動作電流もほぼ一定の直流電流となるため、電源に重畳する雑音も小さくなり発振周波数の安定度が向上すると共に他への電源を介した雑音の影響を小さくすることができる。

【００１４】また、電源間に直列に接続されるトランジスタの数が従来の電圧制御型発振回路と比較して少なくなるので、その分電源電圧を下げることも可能である。電源電圧をさげても前述の通り寄生容量の影響が少ないので高周波発振が可能である。

【００１５】さらに、従来の電圧制御型発振回路のように制御電圧変換回路を必要とせず制御入力端子が一つでよいため、該端子を低インピーダンスで駆動することによって周波数安定度の高い電圧制御型発振回路を容易に実現することができると共に、前述の従来の電圧制御型発振回路のように制御電圧の時間的ずれを発生することもない。したがって、１１の制御入力端子に入力される電圧の時間的変化に対する発振周波数の変化速度も速くなり、ダイナミック特性が向上する。

【００１６】なお、以上述べた実施例は本発明の電圧制御型発振回路の一実施例である。本実施例では１の差動増幅器をＣＭＯＳトランジスタで構成しているが、バイポーラトランジスタで構成してもかまわない。また９および１０の差動入力トランジスタの負荷をトランジスタで構成しているが、単なる抵抗素子で構成してもかまわない。

【００１７】

【発明の効果】以上述べたように本発明の電圧制御型発振回路によれば、従来技術と比較して低電源電圧動作が可能となり、低電源電圧で高周波発振周波数を得ることができるため低消費電力化に効果がある。また、電圧制御型発振回路全体の動作が直流動作に近くなるため、発振周波数の安定度が向上すると共に他の回路への電源を介した雑音の影響を大幅に低減することができる。さらに、周波数制御入力端子が１つであるため、制御電圧変換回路が不要となり回路が簡単になってダイナミック特性も向上する。

【図面の簡単な説明】

【図１】本発明の電圧制御型発振回路の一実施例を示す図。

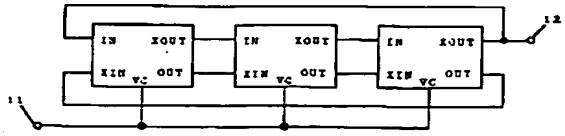
【図２】差動増幅器の構成例を示す図。

【図３】従来の電圧制御型発振回路例を示す図。

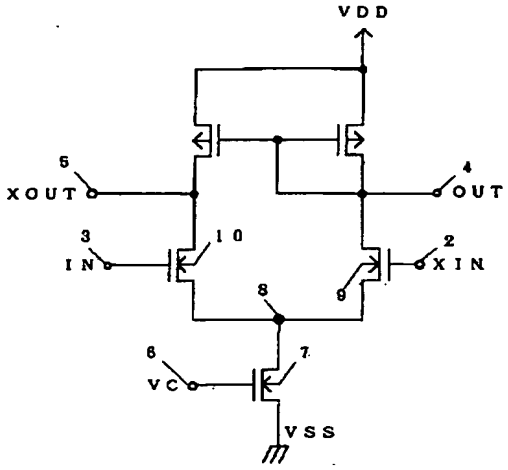
【符号の説明】

１	差動増幅器
２，３	差動入力端子
４，５	差動出力端子
６	電流制御入力端子
７	電流制御トランジスタ
８	７のドレイン端子
９，１０	差動入力トランジスタ
１１	制御入力端子
１２	電圧制御型発振回路の出力端子
２０	制御電圧変換回路
２１，２２	電流制御トランジスタ
２３	２１のドレイン端子
２４	２２のドレイン端子

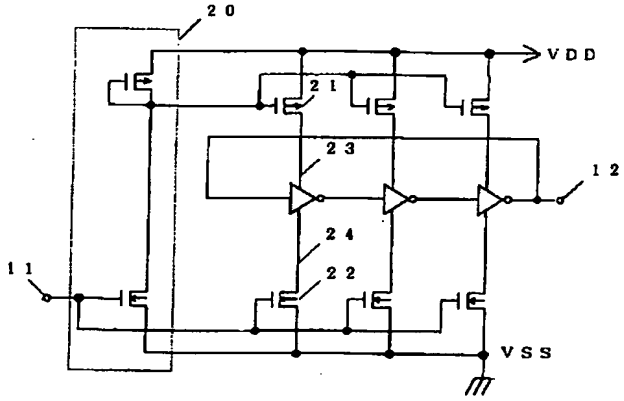
【図１】


IN
XOUT
XIN
VC
OUT
11
12

【図２】


VDD
5
XOUT
4
OUT
3
IN
10
2
XIN
8
9
6
VC
7
VSS

【図３】


20
VDD
21
23
12
24
22
11
VSS

[Name of Document] Specification

[Title of the Invention] A voltage controlled oscillating circuit

[Claims]

[Claim 1]

A voltage controlled oscillating circuit comprising differential amplifiers which have a pair of differential voltage input terminals and a pair of differential voltage output terminals and make the differential output of the amplified output of the differential voltage input onto the differential voltage input terminal to the differential output terminals is proposed. The differential amplifiers have differential amplifiers where the working current of differential amplifying is regulated by the input from a controlled input terminal. The differential amplifiers are connected in series and a ring shape as their working polarity is set opposite of each other of the differential voltage input terminals and differential output terminals of the differential amplifiers which are connected back and forth to one another.

[Claim 2]

A voltage controlled oscillating circuit according to claim 1, wherein current controlled input terminals of the differential amplifier are connected to one another, and the controlled input terminal is designated as an input and any single or multiple output terminals of the differential amplifiers are designated as the output.

[Detailed explanation of the invention]

[0001]

[Industrial Applications]

The present invention is related to a voltage controlled oscillating circuit.

[Prior art technology]

A voltage controlled oscillating circuit of a prior art technology was, for example (as shown in Fig 3), made of an inversion circuit as a ring oscillator, wherein each current controlled transistor was inserted in the VDD side and the VSS side of one inversion circuit and the oscillating frequency was controlled by controlling the currents flowing in two current controlled transistors simultaneously through a controlled voltage input to the controlling input terminal11.

[0003]

The working current of each inversion circuit in the prior voltage controlled oscillating circuit is a function of the input voltage of the inversion circuit, and is not constant. This is obvious from a viewpoint of the working principle of a CMOS inversion circuit. Therefore, the current running in a current controlled transistor 21 and 22 in the oscillating operation is not constant either. The through-current, which is running in the inversion circuit at twice the frequency as the oscillating frequency is supposed to run in a pulse wave. Therefore, the operation of the constant current saturated region is only requested for transistor 21 and 22 at the moment when the pulse current runs, and at the rest of the time, it is in a status of operation of a desaturated region.

[0004]

Looking at 23 and 24, which are the drain terminals of 21 and 22, the terminal voltages should swing with the pulse wave at twice the frequency as the oscillating frequency. In this case, the oscillating frequency is relatively low. There have been no particular problems. However, the following problems have recently been generated, when a higher frequency is required for oscillating.

[0005]

To raise the oscillating frequency at the same controlled voltage, it is necessary to make the working current large by making the current capacity [blank], with the current controlled transistor 21 and 22. But usually, doing this brings an increase in the physical dimensions of the transistor. An increase of the parasitic capacity in 23 and 24 has been made in proportion to this. As mentioned earlier, 23 and 24 have a voltage swing at twice the frequency as the oscillating frequency. Therefore, if the parasitic capacity is large, the parasitic capacity should work to decrease the oscillating frequency to prevent a high-speed voltage change. Judging from what was mentioned above, even if the current capacity of the current controlled transistor is increased to raise the oscillating frequency, the oscillating frequency should be limited and be low, due to the parasitic capacity. Further, because of the current running in the parasitic capacity, a problem also occurred in that the linearity of the oscillating frequency to the working current of the inversion circuit was lost.

[Problems overcome by the invention]

[0006]

Because four (4) transistors are connected in series between the power sources in the prior voltage controlled oscillating circuit, there is a problem in that the voltage of the power source can not be lower than one particular voltage, to secure the voltage between terminals of each transistor. Therefore, it cannot correspond sufficiently to a lower voltage trend of the power source. Moreover, as two current controlled transistors are

used per one inversion circuit, an additional controlled voltage conversion circuit is necessary. This will provide following problems:

[0007]

When an AC signal is input into controlled input 11 of a prior voltage controlled oscillating circuit, the AC signal is transmitted as it is to the gate terminal of a current controlled transistor 22. A lag time of the controlled voltage will be generated between the gate terminals of 22 and 21, because of the signal transmitted to the gate terminal of the current controlled transistor 21 after passing the controlled voltage conversion circuit 20. Even if input 11 is driven with enough low impedance, the output impedance cannot be too small, from a viewpoint of current consumption. Therefore, the output of the controlled voltage conversion circuit 20 is subject to influence by the oscillating and then there is a problem in that it is difficult to increase the stability of the entire oscillating frequency.

[0008]

Moreover, as mentioned previously, because the pulse shaped through-current is running at twice the frequency as the oscillating frequency in each inversion circuit, the higher a oscillating frequency is, the lower impedance of a power source needs to be. Otherwise, there is a problem in that the stability of oscillating is likely to be lost since the other circuit or the circuit itself is influenced by the power source noise with a result of noise being put into the power source.

[0009]

[Problem resolution means]

A voltage controlled oscillating circuit related to the present invention comprises differential amplifiers which have a pair of differential voltage input terminals and a pair of differential voltage output terminals and make the differential output of the amplified output of the differential voltage input onto the differential voltage input terminal to the differential output terminals, wherein the differential amplifiers have differential amplifiers where the working current of differential amplifying is regulated by an input from a controlled input terminal. The differential amplifiers are connected in series and a ring shape as their working polarity is set opposite of each other of the differential voltage input terminals and the differential output terminals of the differential amplifiers which are connected back and forth to one another.
Also, the current controlled input terminals of the differential amplifier are connected to one another, and the controlled input terminal is designated as an input and any output terminals of the differential amplifiers are designated as output.

[0010]

[Embodiment]

An embodiment of the voltage controlled oscillating circuit related to the present invention using 3 differential amplifiers is shown in Fig. 3. 1 is a differential amplifier. An example is shown in Fig,2, in case it is constructed by a CMOS transistor. 2 and 3 are differential input terminals, and 4 and 5 are differential output terminals. 6 is a current controlled input terminal. A voltage input to the terminal controls the working current of the working amplifier. An explanation will be omitted because the operation of this differential amplifier is widely known.

[0011]

In a voltage controlled oscillating circuit in Fig.1, the differential amplifiers are connected in a series and a ring shape, as their working polarity is set opposite to each other of the differential voltage input terminals and differential output terminals of the differential amplifiers which are connected back and forth to one another. And the differential amplifier is connected as to constitute a ring oscillator. Also, the current controlled input terminal of 3 differential amplifiers are connected to each other and constitutes the controlled input terminal 11 of a voltage controlled oscillating circuit. 12 is an output terminal of a voltage controlled oscillating circuit. The output terminal can be any output terminal of any different amplifier constituting a voltage controlled oscillating circuit. Also in Fig. 1, one of output terminals of the differential amplifier is used for single end output, but both of output terminals of the differential amplifier can be used for differential output. Outputs of multiple differential amplifiers can be used for multiple output terminals simultaneously.

[0012]

The working status of the differential amplifier 1 in the oscillating status of a voltage controlled oscillating circuit will be described as follows. In the differential input transistors 9 and 10, current flows corresponding to the input voltage of differential input terminal 2 and 3, and the sum of both currents in the current controlled transistor 7. If the current controlled transistor 7 takes constant current operation in a saturated region by a direct current voltage given in controlled input 6, almost constant direct current should run in current controlled transistor 7. Therefore, the voltage of drain terminal 8 of the current controlled transistor 7 is kept stable, at an almost constant voltage without a sudden transformation in the pulse wave as in a prior voltage controlled oscillating circuit. As to use in a saturated region in the current controlled transistor 7, attempts to optimize between the constitution of differential amplifier 1 and the range of the controlled input voltage is easy because voltage 8 is almost constant.

[0013]

It is not necessary to conduct rapid charge and discharge for the parasitic capacity in terminal 8 as voltage 8 is almost constant. Therefore influence of the parasitic capacity will be minimized. This makes an oscillating frequency higher to the working current running in the current controlled transistor 7 and makes lifts the linearity. Moreover, the noise put on a power source becomes small and the stability of an oscillating frequency is improved, because the working current of the entire voltage controlled oscillating circuit is also almost constant direct current. With this, influence by noise through other power sources can be minimized.

[0014]

As the number of transistors connected in series between the power sources is smaller compared with a prior voltage controlled oscillating circuit, a voltage of a power source can be lowered accordingly. Oscillating with higher frequency is possible as the influence of parasitic capacity by lowering a power voltage, is less likely as mentioned earlier.

[0015]

Further, as there is no need of a controlled voltage conversion circuit as in a prior voltage controlled oscillating circuit. The one controlled input terminal is enough. A voltage controlled oscillating circuit with high stability of frequency is easily achieved by operating the input terminal with low impedance. In addition to this advantage, the time lag of controlled voltage will never occur as in a prior voltage controlled oscillating circuit described previously. Therefore, the dynamic characteristic is also improved as response speed of an oscillating frequency to the time deviation in a voltage input into the controlled input terminal 11 becomes faster.

[0016]

The embodiment mentioned above is just one example of a voltage controlled oscillating circuit related to the present invention. In this example, a CMO transistor is used for differential amplifier 11, but bipolar transistor can be used. Also the load of the differential input transistor 9 and 10 is constituted of transistors, but can be constituted of just a resistance element.

[0017]

[Efficacy of the Invention]

As described above, according to a voltage controlled oscillating circuit related to the present invention, the operation with a lower voltage from the power source is feasible compared with a prior technology. Therefore there is advantage in lowering power consumption as the oscillating frequency with high frequency can be obtained with low voltage from the power source. Also, as an entire operation of a voltage controlled

oscillating circuit is similar to a direct current operation, and stability of oscillating frequency is improved. On top of this, the influence of noise to other circuits through a power source can be reduced greatly. Further, there is no need of a controlled voltage conversion circuit as there is just one frequency controlled input terminal. Therefore, the circuit is made simple and the dynamic characteristic is improved.

[Brief description of drawings]

[Fig.1] A figure showing one example of a voltage controlled oscillating circuit related to the present invention.

[Fig. 2] A figure showing structural example of a differential amplifier

[Fig. 3] A figure showing an example of a prior voltage controlled oscillating circuit.

[Explanations of codes]

1	Differential amplifier
2, 3	Differential input terminal
4, 5	Differential output terminal
6	Current controlled input terminal
7	Current controlled transistor
8	Drain terminal of 7
9, 10	Differential input transistor
11	Controlled input terminal
12	Output terminal of a voltage controlled oscillating circuit
20	Controlled voltage conversion circuit
21, 22	Current controlled transistor
23	Drain terminal of 21
24	Drain terminal of 22

IDS : 8-274592 Abstract

[Title of Invention] A voltage controlled oscillating circuit

[Abstract]

[Objective]

To provide a voltage controlled oscillating circuit to make a stable output of a high frequency oscillation with operation from a low voltage power source.

[Construction]

A voltage controlled oscillating circuit using multiple differential amplifiers. The differential voltage input terminals and the differential output terminals of the differential amplifiers, which are connected back and forth to one another, are connected in a series and a ring shape as their working polarity is set opposite in each other of differential voltage input terminals and differential output terminals of the differential amplifiers. A current controlled input terminal11 of all the differential amplifiers are connected to one another, and constitute a controlled input terminal 11. 12 is the output terminal of a voltage controlled oscillating circuit. Any output terminal of any differential amplifier constituting a voltage controlled oscillating circuit can be used for this output terminal. Also, one of the differential amplifier output terminals is used for single output, but both of the differential output terminals of a differential amplifier can be used for a differential output. The output of multiple differential amplifiers can be used for multiple output terminals simultaneously.